REMARKS

Claims 1 through 16 and 26 through 39 are currently pending in the application.

This amendment is in response to the Office Action of December 17, 2001.

Applicant submits that the objection to the drawings under 37 CFR 1.83(a) has been addressed by amending the specification to state that the "adaptor board 18 includes at least one or more wire bond via 42 which is located in a position or positions aligned with the semiconductor die bond pads 38." Such an arrangement is illustrated in drawing Fig. 3 of the application. Applicant further submits that 35 U.S.C. § 132 has been complied with as no new matter has been introduced into the application.

Claims 1 through 4 and 26 through 29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Eide (U.S. Patent 5,313,096).

Claims 5, 6, 30 and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen (U.S. Patent 5,384,689) in view of Kohno et al. (U.S. Patent 5,293,068).

Claims 8 through 11 and 33 through 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al. (U.S. Patent 5,293,068).

Claims 12, 14 through 16 and 37 through 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Shen (U.S. Patent 5,384,689).

Claims 7 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen (U.S. Patent 5,384,689) as applied to claim 5 above, and further in view of Degani et al. (U.S. Patent 5,473,512).

Claims 13 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) and Shen (U.S. Patent 5,384,689) as applied to claim 12 above, and further in view of Degani et al. (U.S. Patent 5,473,512).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited

prior art for purposes of anticipation. Applicant further submits that the claimed invention is clearly distinguished over any combination of the cited prior art regarding any rejection under the provisions of 35 U.S.C. § 103.

Applicant submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicant submits that the presently claimed invention of claims 1 through 4 and 26 through 29 are clearly not anticipated under 35 U.S.C. § 102(b) as being anticipated by the Eide reference. Applicant submits that the Eide reference does not and cannot anticipate the presently claimed invention of such claims because the Eide reference does not describe each and every element of the identical invention, either expressly or inherently, in as complete detail as is contained in the claim. For instance, the Eide reference does not describe, either expressly or inherently, the presently claimed elements of the claimed invention calling for "providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface" and "providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis

of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface".

In contrast to the presently claimed invention, the Eide reference does not describe whatsoever such a semiconductor die in any fashion. Therefore, claims 1 through 4 and 26 through 29 are not anticipated by the Eide reference under 35 U.S.C. § 102. Accordingly, claims 1 through 4 and 46 through 29 are allowable.

Turning to claims 5, 6, 30 and 31 as being unpatentable under 35 U.S.C. § 103(a) as being unpatentable over the Shen reference in view of the Kohno et al. reference, Applicant submits that the combination of the cited prior art fails to teach or suggest the claimed invention to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the Shen reference in view of the Kohno et al. reference or to combine reference teachings, there has been no showing of a reasonable expectation of success, the combination of the cited prior art references do not teach or suggest all of the claim limitations, and the suggestion to make the claimed combination and the reasonable expectation of success of the combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure, not on the disclosure of the cited prior art.

Applicant submits that there is no suggestion or motivation to combine the Shen and Kohno et al. references whatsoever. While the Shen reference suggests the use of another printed circuit board, there is no suggestion as how such board is to be connected to the printed circuit boards 60 and 70. Only Applicant's disclosure suggests any such configuration of the claimed invention as set forth in claims 5, 6, 30, and 31.

Therefore, the proposed combination of the Shen reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 5, 6, 30, and 31 are allowable.

Applicant further submits that there has been no showing of success for the combination of the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103

regarding the claimed invention whatsoever. The Shen reference is devoid of any description of how to attach an additional printed circuit board and the connection between the semiconductor die and the master board. Solely Applicant's disclosure contains any such suggestion.

Therefore, the proposed combination of the Shen reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 5, 6, 30, and 31 are allowable.

Further, the proposed combination of the cited prior art fails to teach or suggest all the claim limitations of the claimed invention such as those calling for "providing a master board having a plurality of circuit traces thereon", "providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board", "providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board", "attaching said semiconductor die to a portion of the die side surface of the board", "connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the at least one via extending through then board", "connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board", and "wherein the plurality of electrical connectors comprise solder balls".

Applicant submits that solely Applicants disclosure describes such a method, not the cited prior art.

Therefore, the proposed combination of the Shen reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 5, 6, 30, and 31 are allowable.

Finally, Applicant submits that the proposed combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. Such

a hindsight reconstruction of the claimed invention is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Solely, Applicant's disclosure contains the claimed method of the invention.

Therefore, the proposed combination of the Shen reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 5, 6, 30, and 31 are allowable.

Addressing the rejection of claims 8 through 11 and 33 through 36 as being unpatentable under 35 U.S.C. § 103(a) as being unpatentable over the Kryzaniwsky reference in view of the Kohno et al. reference, Applicant submits that such a combination of the cited prior art fail to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the Kryzaniwsky reference in view of the Kohno et al. reference or to combine reference teachings, there has been no showing of a reasonable expectation of success, the combination of the cited prior art references do not teach or suggest all of the claim limitations, and the suggestion to make the claimed combination and the reasonable expectation of success of the combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure, not on the disclosure of the cited prior art.

Applicant submits that there is no suggestion or motivation to combine the Kryzaniwsky and Kohno et al. references whatsoever. While the Kryzaniwsky reference suggests the use of stacked printed circuit boards, there is no suggestion as how such stacked boards are to be connected to another substrate as set forth in the claims. Only Applicant's disclosure suggests any such configuration of the claimed invention as set forth in claims 8 through 11 and 33 through 36.

Therefore, the proposed combination of the Kryzaniwsky reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 8 through 11 and 33 through 36 are allowable.

Applicant further submits that there has been no showing of success for the combination of the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention whatsoever. Neither the Kryzaniwsky reference nor the Kohno et al. reference describes how they may be combined. Solely Applicant's disclosure contains any such suggestion.

Therefore, the proposed combination of the Kryzaniwsky reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 8 through 11 and 33 through 36 are allowable.

Further, the proposed combination of the cited prior art fails to teach or suggest all the claim limitations of the claimed invention such as those calling for "providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface", "providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the substrate", "attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate", and "connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said substrate using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate".

Applicant submits that solely Applicants disclosure describes such a method, not the cited prior art. At best, the Kryzaniwsky reference and the Kohno et al. reference disclose some type of semiconductor chip having bond pads thereon.

Therefore, the proposed combination of the Kryzaniwsky reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 8 through 11 and 33 through 36 are allowable.

Finally, Applicant submits that the proposed combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. Such a hindsight reconstruction of the claimed invention is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Solely, Applicant's disclosure contains the claimed method of the invention.

Therefore, the proposed combination of the Kryzaniwsky reference and the Kohno et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 8 through 11 and 33 through 36 are allowable.

Considering the rejection of claims 12, 14 through 16 and 37 through 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Kryzaniwsky reference in view of the Shen reference, Applicant submits that such claims are allowable as depending from allowable independent claims. Further, Applicant submits that such a proposed combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the Kryzaniwsky reference in view of the Shen reference or to combine reference teachings, there has been no showing of a reasonable expectation of success, the combination of the cited prior art references do not teach or suggest all of the claim limitations, and the suggestion to make the claimed combination and the reasonable expectation of success of the combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure, not on the disclosure of the cited prior art.

Applicant submits that there is no suggestion or motivation to combine the Kryzaniwsky and Shen references whatsoever. While the Kryzaniwsky reference suggests the use of stacked printed circuit boards, there is no suggestion as how such stacked boards are to be connected to

another master board as set forth in the claims. Only Applicant's disclosure suggests any such configuration of the claimed invention as set forth in claims 12, 14 through 16, and 37 through 39.

Therefore, the proposed combination of the Kryzaniwsky reference and the Shen reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 12, 14 through 16, and 37 through 39 are allowable.

Applicant further submits that there has been no showing of success for the combination of the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention whatsoever. Neither the Kryzaniwsky reference nor the Shen. reference describes how they may be combined. Solely Applicant's disclosure contains any such suggestion.

Therefore, the proposed combination of the Kryzaniwsky reference and the Shen reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 12, 14 through 16, and 37 through 39 are allowable.

Further, the proposed combination of the cited prior art fails to teach or suggest all the claim limitations of the claimed invention such as those calling for "[a]master board", "providing a plurality of semiconductor die, each semiconductor die being a semiconductor die having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface", "providing a master board having a plurality of circuit traces thereon", "providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board", "providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board", "attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board", "connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds

extending through the a via extending through then board", and "connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface".

Applicant submits that solely Applicants disclosure describes such a method, not the cited prior art. At best, the Kryzaniwsky reference and the Shen reference disclose some type of semiconductor chip stacking arrangement.

Therefore, the proposed combination of the Kryzaniwsky reference and the Shen reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 12, 14 through 16, and 37 through 39 are allowable.

Finally, Applicant submits that the proposed combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. Such a hindsight reconstruction of the claimed invention is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Solely, Applicant's disclosure contains the claimed method of the invention.

Therefore, the proposed combination of the Kryzaniwsky reference and the Shen reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 12, 14 through 16, and 37 through 39 are allowable. Next, considering the rejection of claims 7 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Shen reference in view of the Degani et al. reference, Applicant submits that such a proposed combination of the cited prior art fails to establish a *prima facie* case of obviousness regarding the claimed invention. Applicant submits that such a combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the Shen reference in view of the

Degani et al. reference or to combine reference teachings, there has been no showing of a reasonable expectation of success, the combination of the cited prior art references do not teach or suggest all of the claim limitations, and the suggestion to make the claimed combination and the reasonable expectation of success of the combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure, not on the disclosure of the cited prior art.

First, Applicant further submits that such claims 7 and 32 are allowable as they depend from allowable independent claims.

Next, Applicant submits that there is no suggestion or motivation to combine the Shen Degani et al. references whatsoever. While the Shen reference suggests the use of a printed circuit board and semiconductor chip, there is no suggestion as how such board is to be connected to another using solder balls as set forth in the claims. Only Applicant's disclosure suggests any such configuration of the claimed invention as set forth in claims 7 and 32.

Therefore, the proposed combination of the Shen reference and the Degani et al. reference reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 7 and 32 are allowable.

Applicant further submits that there has been no showing of success for the combination of the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention whatsoever. Neither the Shen reference nor the Degani et al. reference describes how they may be combined. Solely Applicant's disclosure contains any such suggestion.

Therefore, the proposed combination of the Shen reference and the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 7 and 32 are allowable.

Further, the proposed combination of the cited prior art fails to teach or suggest all the claim limitations of the claimed invention such as those calling for "providing a semiconductor die having a plurality of bond pads thereon", "providing a master board having a plurality of

circuit traces thereon", "providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board", "providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board", "attaching said semiconductor die to a portion of the die side surface of the board", "connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the at least one via extending through then board", "connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board", and "wherein the plurality of electrical connectors comprise solder balls".

Applicant submits that solely Applicants disclosure describes such a method, not the cited prior art. At best, the Shen reference and the Degani et al. reference disclose some type of semiconductor chip having bond pads connected to a substrate and to another board.

Therefore, the proposed combination of the Shen reference and the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 7 and 32 are allowable.

Finally, Applicant submits that the proposed combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. Such a hindsight reconstruction of the claimed invention is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Solely, Applicant's disclosure contains the claimed method of the invention.

Therefore, the proposed combination of the Shen reference and the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 7 and 32 are allowable.

Finally, considering the rejection of claims 13 and 38 as being unpatentable under 35 U.S.C. § 103(a) as being unpatentable over the Kryzaniwsky reference in view of the Shen

reference and in further view of the Degani et al. reference, Applicant submits that such claims are allowable as depending from allowable independent claims. Applicant further submits that such proposed combination of the cited prior art does not establish a *prima facie* case of obviousness regarding the claimed invention because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the Kryzaniwsky reference in view of the Shen reference and the Degani et al. reference or to combine reference teachings, there has been no showing of a reasonable expectation of success, the combination of the cited prior art references do not teach or suggest all of the claim limitations, and the suggestion to make the claimed combination and the reasonable expectation of success of the combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure, not on the disclosure of the cited prior art.

Applicant submits that there is no suggestion or motivation to combine the Kryzaniwsky, Shen, and the Degani et al. references whatsoever. While the Kryzaniwsky reference suggests the use of stacked printed circuit boards, there is no suggestion as how such stacked boards are to be connected to a master board using solder balls as set forth in the claims. Only Applicant's disclosure suggests any such configuration of the claimed invention as set forth in claims 13 and 38.

Therefore, the proposed combination of the Kryzaniwsky reference, Shen reference, and the the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 13 and 38 are allowable.

Applicant further submits that there has been no showing of success for the combination of the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention whatsoever. Neither the Kryzaniwsky reference nor the Shen. reference nor the Degani et al. reference describes how they may be combined. Solely Applicant's disclosure contains any such suggestion.

Therefore, the proposed combination of the Kryzaniwsky reference, the Shen reference, and the the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 13 and 38 are allowable.

Further, the proposed combination of the cited prior art fails to teach or suggest all the claim limitations of the claimed invention such as those calling for "[a]master board", "providing a plurality of semiconductor die, each semiconductor die being a semiconductor die having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface", "providing a master board having a plurality of circuit traces thereon", "providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board", "providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board", "attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board", "connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the a via extending through then board", "connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface", and "wherein said the plurality of electrical connectors comprise solder balls".

Applicant submits that solely Applicants disclosure describes such a method, not the cited prior art. At best, the Kryzaniwsky reference, the Shen reference, and the Degani et al. reference disclose some type of semiconductor chip stacking arrangement and connectors.

Therefore, the proposed combination of the Kryzaniwsky reference, the Shen reference, and the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 12, 14 through 16, and 37 through 39 are allowable.

Finally, Applicant submits that the proposed combination of the cited prior art is a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. Such a hindsight reconstruction of the claimed invention is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Solely, Applicant's disclosure contains the claimed method of the invention.

Therefore, the proposed combination of the Kryzaniwsky reference, the Shen reference, and the Degani et al. reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention. Accordingly, claims 13 and 38 are allowable.

In summary, Applicant submits that claims 1 through 16 and 26 through 39 are clearly allowable over the cited prior art for the reasons set forth herein.

Applicant requests the allowance of claims 1 through 16 and 26 through 39 and the case passed for issue.

Respectfully submitted,

James R. Duzan

James R. Duzan
Attorney for Applicant
Registration No. 28,393
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

FIG. 3 illustrates a third embodiment of the present invention designated as a wire bond style/flip chip attach assembly 300. Components which are common to the previous figures retain the same numeric designation. The assembly 300 comprises an inverted semiconductor die 12 having lower surface 14 with at least one bond pad 38 on the semiconductor die lower surface 14. As illustrated, the bond pads 38 are arranged in two rows extending down the longitudinal axis of die 12 being located transverse to the plane of the page, such an arrangement commonly being used for a "leads over" connection to frame leads extending over the die in its normal, upright position. The semiconductor die lower surface 14 is bonded to the adaptor board upper surface 20 with an insulating, sealing adhesive 40. The adaptor board 18 includes at least one or more wire bond via 42 which is located in a position or positions aligned with the semiconductor die bond pads 38. Each individual wire bond 134 is connected to each corresponding individual semiconductor die bond pad 38. Each wire bond 134 extends from the semiconductor die bond pad 38 to a corresponding bond pad or lead 39 on the adaptor board lower surface 24, which communicates with adaptor board connectors 22 through circuit traces 23. The master board terminals 31 are in electrical communication with at least one adaptor board connector 22 extending substantially perpendicularly from the adapter board lower surface 24. Preferably, a sealant 44 encases the bond wires 134 and seals the wire bond via 42 to prevent contamination and damage to the wire bonds.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A method of electrically connecting a semiconductor die to a substrate, comprising:

providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface [thereon];

providing a substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the substrate;

attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said substrate; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said substrate.

8. (Twice Amended) A method of electrically connecting at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of

said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface [thereon];

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the substrate;

attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said substrate using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate.

12. (Amended) 0A method of electrically connecting a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die being a semiconductor die having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface [thereon];

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the a via extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

26. (Twice Amended) A method of attaching a semiconductor die to a substrate, comprising:

providing <u>one of</u> a semiconductor die having a surface having at least one bond [pads] <u>pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface</u> [thereon];

providing a substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the substrate;

attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said substrate; and

connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate.

30. (Amended) A method of attaching a semiconductor die to a master board, comprising:

providing a semiconductor die having at least one bond pad thereon;

providing a master board having at least one circuit trace thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, at least one circuit, and at least one bond pad located on the second attachment surface of the board;

providing at least one electrical connector for connecting the at least one bond pad located on the second attachment surface of the board to the at least one circuit trace of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of said semiconductor die to said at least one bond pad of said board using at least one wire bond, said at least one wire bond extending through the at least one via extending through then board; and

connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board.

33. (Twice Amended) A method of attaching at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die <u>being one of a semiconductor die</u> having a surface having at least one bond pad <u>extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface</u> [thereon];

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, at least two circuits, and at least two bond pads located on the second attachment surface of the substrate;

attaching the surface having at least one bond pad thereon of a semiconductor die of the at least

two semiconductor die to the die side surface of the substrate having the at least one bond pad of the semiconductor die located over one of the at least two vias extending through the substrate; and

connecting said at least one of each of the semiconductor die to said at least two bond pads of said substrate using at least two wire bonds, at least one wire bond of said at least two wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate.

37. (Amended) A method of attaching a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die <u>being one of a semiconductor die</u> having at least one bond pad <u>extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface</u> [thereon];

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the plurality of vias extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.